## REMARKS

### Pending Claims

Applicants have canceled claims 1 and 13-17 without prejudice or disclaimer. New claims 18-21 are presented for examination.

### Double Patenting

Claim 1 has been canceled thereby rendering moot the rejection under 35 U.S.C. §101.

### 35 U.S.C. §103

Claims 18-21 are patentable over the art of record and in particular Miyawaki et al, U.S. Patent No. 5,752,266 and Kato et al, U.S. Patent No. 6,070,205 which are the references relied upon in the 35 U.S.C. §103(a) rejection that has been overcome by the cancellation of claims 13-17.

Claim 18 sets forth many of the same elements claimed in canceled claims 13 and 14.

Claims 19-21 set forth many of the elements of the claimed combination set forth in canceled claims 15-17,

respectively. Accordingly, examination of claims 18-21 is respectfully requested.

The present invention relates to a data processing system having a data processing unit, a display unit, an image input unit and a synchronous memory (SD RAM 6), respectively, each connected to the data processing unit as shown in Fig. 1, for example. Each unit is accessible to the synchronous memory and has a value for its priority order for access to the synchronous memory.

The data processing unit has a plurality of registers that store an initial set value according to a priority order for each unit or module. The initial set value is set to a timer included in the data processing unit. Assuming that a timer counts down, the timer having the least value at the termination of a previous memory access allows memory access to the synchronous memory. A high priority order is provided to a memory access request which is high in real time processing and a low priority order is provided to an access request which is low in real-time processing. In this way, bus access can be permitted according to real-time processing.

Miyawaki discloses an image decode processing apparatus that includes a data processor, a memory controller 4, a display circuit 3 and a memory 4. Each module can access data to be processed in the memory 4 through the memory controller. Access to the memory is controlled for each module according to a priority order of the module. Thus, the memory access is performed using the priority order set in each module. However, the Miyawaki processor does not disclose or suggest the invention as claimed by Applicants in claims 18-21.

Kato discloses a data processing system having a plurality of bus masters (41, 42) connected with a common bus (Fig. 4), in which a fixed or programmable priority order is provided to each bus master during a predetermined period indicated by a bus cycle counter 119. The bus access request that is issued during the predetermined period is permitted to access the bus according to the priority order. The data processor of Kato permits a bus master to be selected according to a priority order in the predetermined period defined by the bus cycle counter. Accordingly, the reference does not disclose the invention of pending claims 18-21.

Applicants have considered the remainder of the art of record and found that none of the references, whether considered individually or in combination, anticipate or render obvious the invention as claimed in the pending claims 18-21. Accordingly, the pending claims should be found to be allowable over the art of record.

**Conclusion**

In view of the foregoing amendments and remarks, Applicants contend that the above-identified application is now in condition for allowance. Accordingly, reconsideration and reexamination is requested.

Respectfully submitted,

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